

**EXPRESS MAIL NO. EE682466416US**

**ABSTRACT OF THE DISCLOSURE**

**PROCESS FOR FORMING A LOW RESISTIVITY TITANIUM  
SILICIDE LAYER ON A SILICON SEMICONDUCTOR SUBSTRATE  
AND THE RESULTING DEVICE**

A process for forming a low resistivity titanium silicide layer on the surface of a silicon semiconductor substrate. In the process, an effective amount of a metallic element such as indium, gallium, tin, or lead is implanted or deposited on the surface of the silicon substrate. A titanium layer is deposited on the surface of the silicon substrate, and a rapid thermal annealing of the titanium-coated silicon substrate is performed to form low resistivity titanium silicide. In preferred processes, the metallic element is indium or gallium, and more preferably the metallic element is indium. A semiconductor device that has a titanium silicide layer on the surface of a silicon substrate is also provided.

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